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Considerations for Choosing SLC versus MLC Flash

NAND Flash memory technology has evolved since its invention and is now produced in at least four variations that optimize or enhance one or more characteristics—typically at the expense of other characteristics. This paper explains these characteristics and how to evaluate the tradeoffs between them when deciding what type to use for a given application.

The original type NAND is the Single Level Cell (SLC) which stores one bit per internal memory cell. The next type invented was the Multi Level Cell (MLC) which stores two bits per cell. That was followed by NAND devices that could store three bits per cell. Technically, MLC means more than one bit per cell, but the term is popularly used to designate two-bit-per-cell devices, and a new term, TLC (Three Level Cell), has emerged to designate three-bit-per-cell devices. This paper uses the term MLC to mean two bits per cell. TLC NAND has a very limited number of erase cycles and is not discussed further in this paper.

The fourth type of NAND, Enhanced MLC (eMLC), is a two-bit-per-cell device that is selected via a test-screen from standard MLC. It is then personalized during manufacturing with operating parameters that increase the number of erase cycles it can endure, but reduce the duration it will retain what was written (typically from 1 year on standard MLC to 3 months for eMLC). Reducing the retention duration is a very acceptable tradeoff since a higher write rate increases the probability that data is updated before its retention period is exceeded anyway.
The name “eMLC” is not standardized across suppliers, so it is necessary to examine the endurance specification of an MLC device to see if it has enhanced endurance. Similarly, in the rest of this paper, “MLC” is used to mean both standard and enhanced MLC; the context of required endurance can be used to determine which one is more appropriate.

The main operational characteristic differences between SLC and MLC, as well as the cost differences, are summarized below (See Appendix A: MLC vs SLC for more details.)

- SLC is typically specified to endure ~10x more erase/write cycles than MLC.
- MLC erase/write operations are 2x to 4x slower than SLC; reads are slightly slower.
- SLC costs less per performance and endurance, but about twice as much per capacity compared to MLC.

For each application, you must consider all three of the above cost dimensions to determine the best solution. This paper specifically considers an EMC VFCache write-through IO caching solution, although the concepts are also relevant to other types of solutions that leverage Flash technology.

Since Flash is most affected by writes, analyzing the write requirements is the best place to start. The writes to a cache consist of: application writes that already are or should become encached, and writes to install data for application reads that miss in the cache. The smaller the capacity of the cache is (relative to the application’s data set capacity), the higher the cache’s miss rate will be.

A popular workload to accelerate is a transactional database; an industry-constructed representation of such a workload is the TPC-C benchmark. In the TPC-C-like configuration tested, a 1.2TB Oracle 11gR2 database was constructed to simulate a 3,000 warehouse, 90M customer database. The run simulated 150 simultaneous users and achieved over 56K TPM using a dual-socket (eight 2.9GHz cores) server with 12GB of memory and 250GB of VFCache. At this transaction throughput, the VFCache serviced 22K read and 14K write requests per second of 8KB IOs, hence the card was being written at 112 MB/s.

One way to describe the write endurance of a flash card or SSD is by the
total amount data that can be written to the device (for example, Terabytes or Petabyte). However, it is difficult to directly compare that endurance metric across devices of different capacities. A more convenient way to describe device endurance is to normalize it to the capacity of the device and to a standard lifetime; e.g., the number of full capacity “fills per day” the device can sustain for a 5-year lifetime is such a metric. The figure below illustrates the capability of the various flash types in terms of this endurance metric.

The 112 MB/s write rate of the TPC-C-like application above equates to a fill-per-day rate of 39 for a 250GB device. It can be seen from the Figure 1(above) that at this fill rate, the only technology that can satisfy this caching requirement is an SLC technology device.
Example of considering your alternatives

The following example illustrates how to analyze your alternatives. Assume that for the same cost, an MLC card with twice the capacity can be purchased. Although a 2x larger cache likely increases the application’s throughput, a lower bound for the new fill-per-day rate can be calculated using the existing write rate. If the lower-bound rate is not suitable for MLC, there is no need to determine the new write rate.

The same write rate into a 2x larger device halves the fill-per-day rate of that device to 19. That rate is still not suitable for an MLC device, hence the MLC solution is not suitable in this application.

Transactional applications stand to benefit greatly from the VFCache product. For the relatively high write rates generated by such applications, SLC Flash typically offers the best cost and performance solution.
Appendix A: MLC vs SLC

To represent two bits of information, MLC must store four states (00, 01, 10, and 11) within the same range that SLC only needs to store two states (0 and 1). A Flash cell represents a given state by the level of charge it stores on the floating gate of its transistor.

Figure 2: A view of the distribution of cell states across a large population of cells newly written with random data. The dashed lines represent the discrimination boundary between states.

The wear-out mechanism of Flash is the creation of defects within the thin oxide insulator separating the floating gate from the transistor channel. These defects produce two effects that increase with degree of wear: 1) some charge gets trapped by the defects, and 2) it becomes easier to leak charge onto or off of the floating gate. MLC is more sensitive to Flash wear than is SLC because—as can be seen from the diagrams above—there is much less separation between the levels of charge that represent the states. Note also that the distributions are...
narrower for MLC than SLC. SLC can afford to be less precise in its level settings in order to erase and write as fast as possible.

**Bit Error Rate, Retention, and Endurance**

Soft bit failures are an expected occurrence with Flash. A Flash device specifies a maximum bit error rate that the device should not exceed within its specified operating conditions and lifetime. Flash controllers must be designed with sufficient error correction to handle the bit error rate of the Flash devices it supports. Two characteristics of Flash that are dependent on the bit error rate value are its endurance and retention. Retention is the duration that the device retains data with less than the specified bit error rate when read. Endurance, or the wear life, is the number of times the device can be erased and re-programmed, and still meet its retention specification. Retention time depends on the level of leakage within cells, and hence on the amount of wear.

![Retention and Endurance Graph](image)

**Figure 3:** Over time, leakage effects will flatten and shift the population distributions and can produce bit errors.

A shorter retention spec allows a longer endurance spec, and vice-versa. At the system level, a controller design that tolerates a higher bit error rate can (to a point), effectively increase the endurance and/or retention available from a Flash device.

**Performance**

One way to maximize the distance between charge states in an MLC cell is to program that value more accurately. To increase the accuracy, the
program and erase operations must execute more slowly (e.g., one-half to one-quarter the speed of SLC).

The read circuit for Flash only has a binary compare capability; i.e., it can test if the cell’s value is higher than a chosen reference level. This requires that two such compares be performed in sequence (as a binary search of the state boundaries) to decide which of the four levels an MLC cell contains.

**Cost**

Many SLC devices share the same die design with an MLC device; the die can be “trimmed” during manufacturing to set internal operating parameters which personalize the device into MLC or SLC. This means that the per-die cost is the same between MLC and SLC, and since MLC holds twice as many bits, its cost per GB is half that of SLC.
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